

Customer No.: 31561
Application No.: 10/709,090
Docket No.: 12029-US-PA

REMARKS

Present Status of the Application

The Final Action rejected presently-pending claims 1-21 because Examiner assert that Applicant's argument has been addressed in the advisory action.

Discussion of Office Action Rejections

1. In the preliminary amendment filed on April 6, 2006, Applicants have added a new claim (claim 22) to more explicitly describe the present invention. **Applicants think that content of claim 22 may be ignored by Examiner and the Office Action should not be made final. After interviewing with Examiner, Examiner agrees to withdrawal the finality of the Office Action.**

2. The Office Action rejected claims 1-21 under 35 U.S.C. 103(a), as being unpatentable over Jang (U.S. Patent No. 5,734,449). Applicants respectfully traverse the rejections for at least the reasons set forth below.

Independent claim 1 recites the features as follows:

1. A pixel structure, comprising:
 - a scan line, disposed over a substrate;
 - a data line, disposed over the substrate;

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an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;

a plurality of transparent capacitance electrodes, disposed over the substrate, wherein the transparent capacitance electrodes comprises at least a first transparent capacitance electrode and at least a second transparent capacitance electrode disposed above the first transparent capacitance electrode; and

a pixel electrode, disposed over the transparent capacitance electrodes and electrically connected to the active component, wherein the pixel electrode and the transparent capacitance electrodes constitute a multilayer pixel storage capacitor.

(Emphasis added).

Claims 2-9 also recite the similar features.

Independent claim 10 recites the features as follows:

10. A manufacturing method, for a pixel structure, comprising:

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sequentially forming an active component, a scan line and a data line over a substrate, wherein the active component is electrically connected to the scan line and the data line;

forming a plurality of transparent capacitance electrodes over the substrate, wherein the transparent capacitance electrodes comprises at least a first transparent capacitance electrode and at least a second transparent capacitance electrode formed above the first transparent capacitance electrode; and

forming a pixel electrode over the transparent capacitance electrodes, wherein the pixel electrode is electrically connected to the active component, wherein the pixel electrode and the transparent capacitance electrodes constitute a multilayer pixel storage capacitor.

(Emphasis added).

Claims 11-19 also recite the similar features.

Independent claim 20 recites the features as follows:

20. A pixel structure, comprising:
a scan line, disposed over a substrate;

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a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component is electrically connected to the scan line and the data line;

a first transparent capacitance electrode, disposed over the substrate;

a pixel electrode, disposed over the first transparent capacitance electrode and electrically connected to the active component and the first transparent capacitance electrode; and

a second transparent capacitance electrode, disposed between the first transparent capacitance electrode and the pixel electrode, wherein a multilayer pixel storage capacitor is formed by the pixel electrode, the first transparent capacitance electrode and the second transparent capacitance electrode.

(Emphasis added).

Claim 21 also recite the similar features.

Independent claim 22 recites the features as follows:

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22. A pixel structure, comprising:

a scan line, disposed over a substrate;

a data line, disposed over the substrate;

an active component, disposed over the substrate adjacent to an intersection of the scan line and the data line, wherein the active component comprises a gate electrically connected to the scan line, a channel disposed over the gate and a source/drain disposed over the channel and electrically connected to the data line and the pixel electrode;

a protection layer, disposed over the substrate for covering the gate of the active component;

a plurality of transparent capacitance electrodes, disposed over the substrate, the transparent capacitance electrodes comprising at least a first transparent capacitance electrode and at least a second transparent capacitance electrode disposed above the first transparent capacitance electrode, wherein the first transparent capacitance electrode is disposed on the protection layer; and

a pixel electrode, disposed over the transparent capacitance electrodes and electrically connected to the active component, wherein the pixel electrode is electrically connected to the first transparent capacitance electrode such that the transparent capacitance electrodes constitute a multilayer pixel storage capacitor.

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In re U.S. Patent No. 5,734,449 (Column 2, line 66 ~ Column 3, line 6), Jang discloses that " In the liquid crystal display apparatus of the present invention as shown in FIG. 3, lower storage electrode 13' and upper storage electrode 17' of storage capacitor part 100 which is concurrently formed with black matrix 13 of thin film transistor part 50 as material for cutting off light and being conductive, are connected in parallel as shown in FIG. 4, so that the total capacitance increases with the same manufacture area as a conventional one". As discussed by Jang, Applicant finds that the lower electrode 13' and upper storage electrode 17' of storage capacitor part 100 is made of poly-crystalline silicon, metal, silicide having a doping agent or amorphous silicon having a doping agent. In this way, aperture ratio of the LCD apparatus illustrated by Jang is decrease. The larger the area occupied by storage capacitor part 100, the lower the aperture ratio is. Additionally, Jang failed to teach or suggest that the lower electrode 13' and upper storage electrode 17' of storage capacitor part 100 can be made of transparent materials. Obviously, the concept of transparent capacitance electrode is "NOT" proposed by Jang to enhance aperture ratio of the LCD apparatus. Therefore, Applicant considers that Claims 1-21 are patently distinguished from US Patent No. 5,734,449.

In the claimed invention, the aperture ratio is not affected by the area occupied by the storage capacitor (i.e. area of transparent capacitance electrodes) even the transparent capacitance electrodes of the storage capacitor occupy almost region under the pixel

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electrode. Accordingly, flexibility of layout design can be improved by the present invention significantly.

In re Column 2, line 66 ~ Column 3, line 6 of U.S. Patent No. 5,734,449, Jang teaches that "lower storage electrode 13' and upper storage electrode 17' of storage capacitor part 100 which is concurrently formed with black matrix 13 of thin film transistor part 50 as material for cutting off light and being conductive". Obviously, Jang teaches away that the lower electrode 13' and upper storage electrode 17' can be formed of transparent conductive materials such as ITO and IZO. Additionally, there is no evidence provided by the Examiner to prove that the capacitor electrode formed of ITO or IZO is obvious. Therefore, Applicant considers that the Examiner fails to establish Prima Facie Case of obviousness and Claims 1-21 are patentable over US Patent No. 5,734,449.

In conventional transmissive LCD panels, the aperture ratio is related with the area occupied by scan lines, data lines, storage capacitors, and other light-shielding metals. The aperture ratio of transmissive LCD panels is highly concerned by one skilled in the art. Jang disclosed a solution to increase the aperture ratio of transmissive LCD panels by providing a storage capacitor having three-layered electrode (13', 17', 19). Substantially, Jang want to reduce the area occupied by the storage capacitance part (Column 3, 62-67) because light from backlight unit will be inherently cut off by the upper storage electrode 17'. Contrary to the Jang's disclosure, the area occupied by the first transparent capacitance electrode and the

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second transparent capacitance electrode of the claimed pixel structure can be very large. In one word, Jang suggested to reduce the area occupied by the storage capacitance part (Column 3, 62-67) to increase aperture ratio, while the present invention suggest to make the capacitance electrode transparent and increase the area occupied by the capacitance electrode to increase aperture ratio. Therefore, the way to increase the aperture ratio of transmissive LCD panels of the present invention is quite different from that disclosed by Jang.

To more explicitly describe the present invention, Applicants have added claim 22 to emphasize the feature "the first transparent capacitance electrode is disposed on the protection layer". In other words, Applicants have emphasized that the first transparent capacitance electrode is located between two different layers. The content of claim 22 is fully support by the specification (see figures 2H and 3F). Specifically, the gate of the active component is covered by the protection layer while the first transparent capacitance electrode is disposed on the protection layer. However, in the US Patent No. 5,734,449, Jang fail to disclose the feature "the first transparent capacitance electrode is disposed on the protection layer". In contrast, Jang discloses that the upper storage electrode 17' and the gate electrode 17 are formed simultaneously.

Jang not only fails to disclose the first transparent capacitance electrode and the second transparent capacitance electrode, but also fails to disclose the manufacturing process as claimed in claim 10. Specifically, the active component and the capacitance

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electrode are formed simultaneously in the US Patent No. 5,734,449, while the active component and the transparent capacitance electrode are formed by different steps.

According to MPEP 2143.03 (All Claim Limitations Must Be Taught or Suggested), Applicants think that “to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)”, however, Jang failed to disclose that the lower electrode 13’ and upper storage electrode 17’ can be formed of transparent conductive materials such as ITO and IZO. In other words, Applicants thinks that the Examiner fails to establish prima facie obviousness of a claimed invention because not all the claim limitations is taught or suggested by Jang. Additionally, According to MPEP 2143.03, Applicants think that “all words in a claim must be considered in judging the patentability of that claim against the prior art.” In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). The word “transparent” in “transparent capacitance electrodes” is not fully considered in judging the patentability of that claim against the prior art.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 10, 20 and 22 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-9, 11-19 and 21 patently define over the prior art as well.

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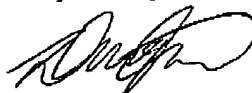
CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-22 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,



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